IN THE SPECIFICATION:

Please amend the paragraph beginning at page 3, line 9, and ending at page 3, line 23, as follows:

--Now, although many improvements have been made in the aforesaid conventionally structured recording head and the aforesaid electro-thermal conversion element driving semiconductor device, recently the following properties of these products have further been required: being capable of being driven in high speed, using less energy, being highly integrated, being manufactured at low costs, and having high properties. In particular, the high density integration of switching devices has been insufficient in conventional head structures. Moreover, it has been easy to happen the rise of a substrate potential (latch up) caused by the lowness of the breakdown voltages of the conventional head structures can easily occur in operation.--

Please amend the paragraph beginning at page 5, line 6, and ending at page 6, line 8, as follows:

--The aforesaid first object of the present invention is achieved by a semiconductor device comprising: a plurality of electro-thermal conversion elements; and a plurality of switching devices for flowing electric currents through the plural electro-thermal conversion elements, wherein: the electro-thermal conversion elements and the switching devices are integrated on a first conductive type semiconductor substrate; the switching devices are insulated gate type field effect transistors that severally include: a second conductive type first semiconductor region formed on one principal surface of the semiconductor substrate; a first conductive type second semiconductor region for supplying a channel region, the second semiconductor region being formed to adjoin the first semiconductor region; a second conductive type source region formed on the surface side of the second semiconductor region; a second conductive type drain region formed on the

surface side of the first semiconductor region; and gate electrodes formed on the channel region with a gate insulator film put between them; and the second semiconductor region is formed by a semiconductor having ~~a~~ an impurity concentration higher than that of the first semiconductor region, the second semiconductor region being disposed between two of the drain regions arranged side by side so as to separate the drain regions in a traverse direction.--

Please amend the paragraph beginning at page 7, line 9, and ending at page 7, line 13, as follows:

--The insulated gate type field effect transistors severally preferably ~~comprises~~ comprise a first conductive type diffusion layer for pulling out an electrode such that the diffusion layer penetrates the source region.--

Please amend the paragraph beginning at page 7, line 19, and ending at page 7, line 22, as follows:

--The first semiconductor region is preferably a well formed by ~~introduce of~~ introducing a reverse conductive type impurity from a surface of the semiconductor substrate.--

Please amend the paragraph beginning at page 7, line 23, and ending at page 7, line 27, as follows:

--The first semiconductor region is preferably composed of a plurality of wells formed by ~~introduce of~~ introducing a reverse conductive type impurity from a surface of the semiconductor substrate and by transversal separation at every drain region.--

Please amend the paragraph beginning at page 8, line 10, and ending at page 8, line 14, as follows:

--The drain sides of the gate electrodes are preferably formed on insulator films thicker than the gate insulator film, and the drain region preferably aligns itself with end portions of the thicker insulator films.--

Please amend the paragraph beginning at page 8, line 15, and ending at page 8, line 20, as follows:

--The second semiconductor region, the source region and the drain region preferably have sectional structures symmetrical on its right side and on its left side, the structures being formed by ~~introduce of~~ introducing impurities by oblique ion implantation.--

Please amend the paragraph beginning at page 10, line 19, and ending at page 10, line 27, as follows:

--Here, it is preferable for the method to comprise the steps of: performing a first conductive type ion implantation into at least a channel region put between the source region and the semiconductor layer on the surface side of the semiconductor region through the gate electrode after the step of forming the semiconductor region; and performing a heat treatment for activating the implanted impurity electrically.--

Please amend the paragraph beginning at page 11, line 1, and ending at page 11, line 11, as follows:

--It is also preferable for the method to ~~comprises~~ comprise the steps of: performing a first conductive type ion implantation into at least a channel region put between the source region and the semiconductor layer on the surface side of the

semiconductor region through the gate electrode after the step of forming the semiconductor region; and performing a heat treatment for activating the implanted impurity electrically, wherein the ion implantation is ion implantation in which ions of boron are implanted in energy of 100 keV or more.--

Please amend the paragraph beginning at page 26, line 2, and ending at page 26, line 4, as follows:

--In the following, the attached drawings are ~~referred~~ referenced while the preferred embodiments of the present invention are described in detail.--

Please amend the paragraph beginning at page 26, line 6, and ending at page 26, line 9, as follows:

--At first, Figs. 1 to 4 are ~~referred~~ referenced while a semiconductor device for a liquid jet apparatus according to Embodiment 1 of the present invention is described in detail.--

Please amend the paragraph beginning at page 28, line 15, and ending at page 29, line 8, as follows:

--An outline of the operation of the semiconductor device is described. A reference voltage such as, for example, a ground potential is given to the p-type semiconductor substrate 1 and the source regions 7. Then, the high reference voltage VDD is supplied to one side terminals of the electro-thermal conversion elements 31 to 33. When an electric current is ~~flown~~ flowed through only, for example, the electro-thermal conversion element 31 among them, by the turning on of only a switch 34, a gate voltage VG is supplied to the gate electrodes 4 of the transistors of the two segments constituting the switching device Tr1 to turn on the switching device Tr1. Then, an electric current flows ~~form~~ from the power source

terminal to the grounded terminal through the electro-thermal conversion element 31 and the switching device Tr1 to generate heat in the electro-thermal conversion element 31. Then, as it is well known, the heat is utilized to jet liquid.--

Please amend the paragraph beginning at page 35, line 23, and ending at page 36, line 15, as follows:

--Next, as shown in Fig. 6D, a heat treatment is performed at 1100°C for 60 minutes in an electric furnace to form the base region 6 to be about 2.2 mm in depth for the traverse electrical separation of the well region 2. In the present embodiment, it is important to design the base region 6 to be deeper than the well region 2 for the complete separation of the well region 2 by the heat treatment, and the conditions of the heat treatment ~~is~~ are determined according to the depth of the well region 2, the concentration thereof, the kind of the impurity thereof, and the concentration and the kind of the impurity of the impurity layer 205. The depth of the base region 6 used in the present invention can be selected in a range of, for example, about from 1 mm to 3 mm, and the concentration of the base region 6 can be selected in a range of, for example, about from $1 \times 10^{15}/cm^3$ to $1 \times 10^{19}/cm^3$ at the most outside surface.--

Please amend the paragraph beginning at page 36, line 16, and ending at page 36, line 23, as follows:

--Next, as shown in Fig. 6E, the source region 7, a first drain region 8 and a second drain region 9 are formed by the ion implantation of, for example, arsenic by the use of gate electrodes 4 as masks. Thus, the source region 7 and the drain regions 8 and 9 are formed ~~with~~ overlapping with each other a little while self-adjusting with the gate electrodes 4.--

Please amend the paragraph beginning at page 38, line 2, and ending at page 38, line 13, as follows:

--Because the base region 6, the source region 7 and the drain regions 8 and 9 are formed by the use of the gate electrodes 4 as the mask for ion implantation, those regions 6, 7 and 8 are formed ~~with~~ while being adjusted to the gate electrodes 4, and consequently the high integration of the switching device array and the equalization of the characteristics of each device can be achieved. Moreover, because the source region 7 and the domain regions 8 and 9 are formed in the same process, the embodiment contributes to the suppression of manufacturing costs.--

Please amend the paragraph beginning at page 39, line 24, and ending at page 39, line 27, as follows:

--Figs. 8A to 8G are ~~referred~~ referenced while the manufacturing process of a semiconductor device according to Embodiment 4 of the present invention is described.--

Please amend the paragraph beginning at page 41, line 11, and ending at page 42, line 8, as follows:

--Next, a (not shown) pad oxide film is grown to be 10 nm in thickness by, for example, pyrogenic oxidation on the surface of the well region 2. A (not shown) silicon nitride film is deposited on the pad oxide film to be 150 nm in thickness by, for example, LPCVD method. Then, patterning is performed by photolithography to etch the silicon nitride film. After that, field insulator films 221 are selectively grown to be 500 nm in thickness by, for example, the pyrogenic oxidation. After that, the silicon oxide film is completely removed by the use of, for example, phosphoric acid, and the pad oxide film is removed by, for example, the 10 wt% of a hydrogen fluoride solution. Then, the gate insulator films 203 are grown to be 10 nm in thickness on the n-type well region 2 by, for

example, the pyrogenic oxidation. At this time, although the aforesaid pad oxide film can be used as the gate insulator films 203 as it is, it is not preferable with respect to its reliability. Thus, as shown in Fig. 8B, the gate insulator films 203 as thin oxide ~~film~~ films and the field insulator films (field oxide films) 221 as thick oxide films are disposed at desired positions on the n-type well regions 2.--

Please amend the paragraph beginning at page 43, line 7, and ending at page 43, line 20, as follows:

--Next, as shown in Fig. 8E, a heat treatment is performed, for example, at 1100°C for 60 minutes with an electric furnace to form the base region 6 for the traverse electrical separation of the well region 2. In the present embodiment, it is important to design the heat treatment such that the base region 6 becomes deeper than the well region 2 for the complete separation of the well region 2 by the base region 6 in the vertical direction, and it is desirable to design the heat treatment such that the base ~~regions~~ region 6 is situated at a position near to the boundaries between the gate insulator films 203 and the field insulator 221 in the transverse direction.--

Please amend the paragraph beginning at page 44, line 16, and ending at page 44, line 27, as follows:

--Next, as shown in Fig. 8F, the source region 7, a first drain region 8 and a second drain region 9 are formed by, the ion implantation of, for example, arsenic. At this time, the gate electrodes 4 ~~functions~~ function as the masks that regulate the end portions of the source electrode 7, and the field insulator films 221 function as the masks that regulate the end portions of the drain regions 8 and 9. Thus, the source region 7 self-adjusts with gate electrodes 4 and the drain regions 8 and 9 self-adjust with the filed insulator films 221.--

Please amend the paragraph beginning at page 51, line 24, and ending at page 52, line 4, as follows:

--The structure of the MIS type field effect transistor is different from the structure of the usual one. In the present structure, a channel is formed in a drain for enabling the drain that determines the breakdown voltage of the transistor to be made deeper and ~~low concentrated~~ of lower concentration. Consequently, the breakdown voltage thereof can be improved.--

Please amend the paragraph beginning at page 52, line 24, and ending at page 53, line 11, as follows:

--On the other hand, according to the semiconductor devices of respective embodiments mentioned above, their drain concentrations can be set to be lower than their channel concentrations, and their drains can be formed to be sufficiently deep. Consequently, the semiconductor devices can have high breakdown voltages and can flow large electric currents. Furthermore, they can operate at high speed owing to their low on-resistances, and then they can realize to be highly integrated and to save energy. Moreover, in a semiconductor device requiring an array-like structure of a plurality of transistors, the semiconductor devices according to the respective embodiments ~~makes~~ make it easy to isolate respective devices.--

Please amend the paragraph beginning at page 54, line 26, and ending at page 55, line 15, as follows:

--In the aforesaid semiconductor device and a manufacturing method of the same, the drain concentration thereof can be set to be lower than the channel concentration thereof, and the drain can be formed to be sufficiently deep. Consequently, the semiconductor device has a high breakdown voltage, which enables a large current flow.

Moreover, the semiconductor device has a low on-resistance, which enables the high speed operation thereof. Furthermore, the high integration thereof and the low consumption energy thereof can be realized. Moreover, by the formation of a low concentration p-type well region around the source region 7, isolation between devices ~~becomes~~ is ensured even in a semiconductor device ~~requires~~ requiring an array structure composed of a plurality of transistors.--

Please amend the paragraph beginning at page 56, line 27, and ending at page 57, line 21, as follows:

---In the present embodiment, the low concentration p-type well region 29 is deeply formed to separate the low concentration n-type well region 22, which has been formed sufficiently deeply in advance, in the traverse directions. The base region 26 is formed in the low concentration p-type well region 29. The p-type well region 29 and the ~~baser~~ base region 26 respectively perform the roles of the drain and the channel of an MIS type field effect transistor. Then, it is possible to set the drain concentration lower than the channel concentration. The breakdown voltage of a transistor is determined by the breakdown voltage of the drain. The breakdown voltage of a transistor usually becomes higher, as the drain concentration is lower and the drain depth is deeper. Consequently, the rated voltage of the transistor can be set higher, and the largeness of the electric current flowing the transistor can be enlarged, and further the high speed operation thereof can be realized.--

Please amend the paragraph beginning at page 58, line 7, and ending at page 59, line 7, as follows:

--Figs. 18A to 18F are ~~referred~~ referenced while a manufacturing process of the semiconductor device according to the present embodiment is described. The method

for manufacturing the semiconductor device is roughly a method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of switching devices for flowing electric currents through the plural electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, the method comprising the steps of: forming a second conductive type semiconductor layer on a principal surface of the first conductive type semiconductor substrate 1 (Fig. 18A); forming a gate insulator film 203 on the semiconductor layer (Fig. 18B); forming gate electrodes 4 on the gate insulator film 203 (Fig. 18B); doping a first conductive type impurity by utilizing the gate electrodes 4 as masks (Fig. 18C); forming a semiconductor region by diffusing the first conductive type impurity (Fig. 18D); and forming a second conductive type source region 7 on a surface side of the semiconductor region by utilizing the gate electrodes 4 as masks and second conductive type drain regions 8 and 9 on a surface side of the second conductive type semiconductor layer (Fig. 18E).--

Please amend the paragraph beginning at page 60, line 10, and ending at page 60, line 19, as follows:

--Next, ~~not shown~~ a photoresist (not shown) is coated, and the patterning of the photoresist is performed by the photolithography to remove the photoresist only in the region for the formation of the base region 26 (or the impurity layer 205). Then, as shown in Fig. 18C, the selective ion implantation of a p-type impurity, for example, boron is performed to form the impurity layer 205 by the use of the photoresist (not shown) and the gate electrodes 4 as masks.--

Please amend the paragraph beginning at page 60, line 20, and ending at page 61, line 4, as follows:

--Next, as shown in Fig. 18D, a heat treatment is performed at, for example,

1100°C for 60 minutes in an electric furnace to form the base region 26. It is important to design the base region 26 to form a desired effective channel length in order not to raise the on-resistance of the base region 26 by the heat treatment, and the conditions of the heat treatment ~~is~~ are determined according to the depth of the p-type well region 29, the concentration thereof, the kind of the impurity, and the concentration and the kind of the impurity of the impurity layer 205.--

Please amend the paragraph beginning at page 67, line 3, and ending at page 67, line 11, as follows:

--Next, ~~not shown~~ a photoresist (not shown) is coated. Then, the patterning thereof is performed by the photolithography to remove only the resist in the region to be formed as the base region 26 (or the impurity layer 205). Then, as shown in Fig. 20D, the impurity layer 205 is formed by the selective ion implantation of a p-type impurity, for example, boron by using the photoresist (not shown) and the gate electrodes 4 as masks.--

Please amend the paragraph beginning at page 68, line 27, and ending at page 70, line 7, as follows:

--Next, ~~not shown~~ a photoresist (not shown) is coated, and the patterning thereof is performed by the photolithography. Then, the resist in the region to be formed as the diffusion layer 10 for taking out the base electrodes 4 is removed. After that, as shown in Fig. 20G, the diffusion layer 10 for taking out the base electrodes 4 is formed by, for example, the ion implantation method. Although the diffusion layer 10 for taking out the base electrodes 4 is not always necessary, it is preferable to form the diffusion layer 10 on the designing of the circuit. Moreover, when a p-type MIS type field effect transistor is made at the same time for a signal processing circuit, there is no necessity for increasing the number of processes. After that, the heat treatment is performed for, for example, thirty

minutes at 950°C, and then the source region 7, the first drain region 8, the second drain region 9 and the diffusion layer 10 for taking out the base electrodes 4 are activated. Thus, the insulators on the drain side under the gate electrodes 4, where the electric field concentrates, are formed by the field insulator films 221, and thereby the breakdown voltage between the gates and the drains of the MIS type field effect transistor can be improved. For example, in the case where a complementary MIS type field effect transistor that requires high speed operation is formed on the same substrate where MIS type field effect transistor that requires a high breakdown voltage is formed at the same time, the insulators can be formed without any additional process. Consequently, the formation of the field insulator films 221 is very effective.--

Please amend the paragraph beginning at page 73, line 19, and ending at page 74, line 7, as follows:

--As described above, according to Embodiments 7 to 12 of the present invention, their drain concentrations can be set to be lower than their channel concentrations, and their drains can be formed to be deeper. Consequently, the semiconductor devices can have high breakdown voltages and can flow large electric currents. Furthermore, they can operate at high speed owing to their low on-resistances, and then they can realize ~~to be highly integrated and to save energy~~ high integration and energy conservation. Moreover, in a semiconductor device requiring an array-like structure of a plurality of transistors, the semiconductor devices according to the respective embodiments ~~makes~~ make it easily possible to isolate respective devices without any rise of costs.--

Please amend the paragraph beginning at page 74, line 8, and ending at line 22, as follows:

--Incidentally, in Embodiments 7 to 12, as a measure against the case where the n-type well region 22 is formed deeply, the p-type well region 29 is formed by ~~the introduce of~~ introducing an impurity and after that the base region 26 is formed in another process. When the deeper n-type well region 22 is not necessary, by the separate formation of the n-type well region 22 in the traverse direction at every drain, the base region 26 adjoins to the p-type substrate 1 at the upper part of the substrate 1 remaining between two adjoining n-type wells even if the base region 26 is not formed to be deeper than the n-type well region 22. Consequently, the base region 26 and the substrate 1 can be made to be at the same electric potential.--

Please amend the paragraph beginning at page 81, line 19, and ending at page 82, line 10, as follows:

--The manufacturing method of a semiconductor device according to the present embodiment injects an impurity at the critical angle to the channeling at the time of forming the base region 6, the source region 7, and the drain region 8, as shown in Figs. 27 and 28, while rotating the substrate 1 (wafer 121) in the outer periphery direction of the substrate 1. Consequently, the positional relation between the end face of the base region 6 formed by ~~the~~ introducing ~~of~~ an impurity by the ion implantation and by the thermal diffusion of the implanted impurity and the end faces of the source region 7 and the drain region 8 formed by the same introducing of an impurity by the ion implantation and by the thermal diffusion of the implanted impurity can be formed in a well controlled state no matter how the transistors are arranged on the principal surface of the semiconductor substrate 1.--

Please amend the paragraph beginning at page 87, line 27, and ending at page 88, line 16, as follows:

--Next, as shown in Fig. 30D, a heat treatment is performed at, for example, 1100°C for 60 minutes in an electric furnace to form the base region 6 to separate the well region 2 in a traverse direction electrically. It is preferable to design the heat treatment such that the base region 6 is formed to be deeper than the well region 2 for the complete separation of the well region 2, and the conditions of the heat treatment ~~is~~ are determined according to the depth of the well region 2, the concentration thereof, the kind of the impurity thereof, and the concentration and the kind of the impurity of the impurity layer 205. Here, the structure in which the base region 6 reaches the p-type semiconductor substrate 1 is shown, but the structure of the base region 6 is not limited to such a structure.--

Please amend the paragraph beginning at page 91, line 15, and ending at page 92, line 12, as follows:

--Next, a (not shown) pad oxide film is grown to be about 10 nm in thickness by, for example, pyrogenic oxidation on the surface of the well region 2. A (not shown) silicon nitride film is deposited on the pad oxide film to be 150 nm in thickness by, for example, LPCVD method. Then, patterning is performed by the photolithography to etch the silicon nitride film. After that, field insulator films 221 are selectively grown to be 500 nm in thickness by, for example, the pyrogenic oxidation. After that, the silicon oxide film is completely removed by the use of, for example, phosphoric acid, and the pad oxide film is removed by, for example, the 10 wt% of a hydrogen fluoride solution. Then, the gate insulator films 203 are grown to be 10 nm in thickness on the n-type well region 2 by, for example, the pyrogenic oxidation. At this time, although the aforesaid pad oxide film can be used as the gate insulator films 203 as it is, it is not preferable with respect to its

reliability. Thus, as shown in Fig. 31B, the gate insulator films 203 as thin oxide ~~film~~ films and the field insulator films 221 as thick oxide films are disposed at desired positions on the n-type well regions 2.--

Please amend the paragraph beginning at page 93, line 14, and ending at page 94, line 21, as follows:

--Next, as shown in Fig. 31E, a heat treatment is performed, for example, at 1100°C for 60 minutes in an electric furnace to form the base region 6 for the traverse electrical separation of the well region 2. It is desirable to design the heat treatment such that the base region 6 becomes deeper than the well region 2 for the complete separation of the well region 2 by the base region 6 in the vertical direction, and it is desirable to design the heat treatment such that the base ~~regions~~ region 6 is situated at a position near to the boundaries between the gate insulator films 203 and the field insulator 221 in the transverse direction. The reason is that, if the base region 6 is formed only to the half way of the gate insulator films 203, there is the possibility that the electric field to be generated under the gate electrodes 4 concentrates to the thin gate insulator films 203 to destroy the gate insulator films 203. Moreover, if the base region 6 is formed up to the thick field insulator films 221, the base regions 6 under the thick field insulator films 221 are not inverted even if a predetermined voltage is applied to the gate electrodes 4, and it becomes difficult ~~that~~ for the base regions 6 to perform the switching function of the MIS type electric field transistor. Consequently, even if the switch is turned on, the drivability ability thereof is greatly deteriorated. Accordingly, the conditions of the aforesaid heat treatment is determined according to the depth of the well region 2, the concentration thereof, the kind of the impurity thereof, the concentration and the kind of the impurity of the impurity layer 205 and the sizes of the masks.--

Please amend the paragraph beginning at page 96, line 6, and ending at page 96, line 18, as follows:

--As described above, according to Embodiments 13 to 15, because the ion implantation of the impurity is performed while the substrate 1 is rotated at the time of the formation of at least one of the base ~~region 7~~ region 6, the source region 7 and the drain regions 8, 9, in a semiconductor device requiring an array structure composed of a plurality of transistors, the device structures of both side transistors having a commonly pulled out source electrode put between them can be formed as the same and symmetrical structures, and their threshold voltage and on-resistances at operation can accurately be formed to their designed values.--

Please amend the paragraph beginning at page 102, line 14, and ending at page 103, line 4, as follows:

--That is, when the array arrangement of the MIS type field effect transistors having drains commonly is employed, as shown in Figs. 32 and 33, after the formation of the well regions 2, the base region 6, the gate electrodes 4 and the photoresist masks 211 on the semiconductor substrate 201 including a principal surface having the plane direction inclining (e.g. q = 4°) to a lower dimensional plane direction, the performance of ion implantation 413 into a principal surface perpendicularly in the direction from the gate electrode 4 to the drain or the source enables the uniform ion implantation on the right side and on the left side to the masks. Consequently, the effective channel lengths of adjoining two MIS type field effect transistors become the same (even if there are ~~a little~~ little errors, the lengths can be regarded as the same).--

Please amend the paragraph beginning at page 106, line 14, and ending at page 106, line 23, as follows:

--Electro-thermal conversion elements (heaters) for jetting ink from an exhaust port 53 with air bubbles produced by the heat generated by electric currents flowing through the elements are arranged in a plurality of rows on a device substrate 52 on which the circuit of Fig. 34 are formed. A wiring electrode 54 is provided to each electro-thermal conversion element 41, and ~~on~~ one end side of the wiring electrode 54 is electrically connected with the switching device 42 in the array 42.--

Please amend the paragraph beginning at page 109, line 12, and ending at page 109, line 19, as follows:

--Although the present invention has been described in its preferred form with a certain degree of particularity, obviously many changes and variations are possible therein. It is therefore to be understood that the present invention may be practiced differently than as specifically described herein without departing from scope and the sprit thereof.--